

UTILITY SERIAL NUMBER	PATENT DATE		PATENT NUMBER
SERIAL NUMBER 08/965,286	FILING DATE 11/06/97 RULE 60	CLASS 438 251	SUBCLASS 553 565
			GRANB ART UNIT 1987 2011-2815
APPLICANTS	EXAMINER NADAV		

TAKAYUKI GOMI, TOKYO, JAPAN; HIROAKI AMMO, KANAGAWA, JAPAN.

CONTINUING DATA***

VERIFIED THIS APPLN IS A DIV OF 08/762,779 12/10/96, NOW US. Pat. No.

O.N.

5,976,940

FOREIGN APPLICATIONS***

VERIFIED JAPAN P07-322962

12/12/95

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CPA CPA

Foreign priority claimed 35 USC 119 conditions met	<input type="checkbox"/> yes <input checked="" type="checkbox"/> no <input type="checkbox"/> yes <input checked="" type="checkbox"/> no	AS FILED →	STATE OR COUNTRY JPX	SHEETS DRWGS. 24	TOTAL CLAIMS 10	INDEP. CLAIMS 3	FILING FEE RECEIVED \$790.00	ATTORNEY'S DOCKET NO. P97.2608
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Verified and Acknowledged Examiner's Initials
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TITLE BIPOLAR TRANSISTOR AND METHOD OF MAKING THE SAME SEMICONDUCTOR DEVICE
INCLUDING HIGH SPEED TRANSISTORS AND HIGH VOLTAGE TRANSISTORS
DISPOSED ON A SINGLE SUBSTRATE

U.S. DEPT. OF COMM./PAT. & TM—PTO-436L (Rev.12-94)

PARTS OF APPLICATION FILED SEPARATELY		Applications Examiner	
NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Total Claims	Print Claim
		Assistant Examiner	
ISSUE FEE		DRAWING	
Amount Due	Date Paid	Sheets Drwg.	Figs. Drwg.
		Print Fig.	
Label Area		ISSUE BATCH NUMBER	
		Primary Examiner	
		PREPARED FOR ISSUE	
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Form PTO-436A
(Rev. 8/92)

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